Call For Papers

ABOUT EPTC

The 28th IEEE Electronics Packaging Technology Conference (EPTC2026) is an international event organized by the IEEE RS/EPS/EDS Singapore Joint Chapter and co-sponsored by the IEEE Electronics Packaging Society (EPS). Since its inauguration in 1997, EPTC has established itself as a highly reputable international conference and serve as the IEEE EPS flagship conference in the Asia and Pacific Region. EPTC covers the complete spectrum of electronics packaging technology, from design through final reliability testing, addressing current challenges and future directions in advanced packaging. The conference brings together researchers, industry leaders, and practitioners from around the world to share innovations and best practices across the packaging ecosystem.

The EPTC technical program committee, comprising more than 100 experts from diverse semiconductor packaging technology domains, is committed to creating an engaging technical program for the international packaging community. The technical program will feature keynote addresses, technical sessions, invited talks, panel discussions, workshops, exhibitions, and extensive networking opportunities. In addition to the technical program, the conference will host an industrial exhibition, offering leading companies a valuable platform to showcase their latest technologies and products. In 2025, EPTC attracted more than 800 attendees, and participation is expected to grow further in 2026. EPTC 2026 will be held as a four-day program from 1–4 December 2026, continuing its tradition as a premier forum for technical exchange, industry engagement, and professional networking in electronics packaging.

CONFERENCE TOPICS

You are invited to submit abstract(s) on new research findings and developments in the following packaging topics:

1. Advanced Packaging: Primary focus of this technical domain on packaging system, architecture and application driven topics. System-level architectures including chiplets, 2.5D/3D/3.5D integration, SiP, heterogeneous integration using interposers (Si, RDL, organic, SiC) and silicon bridge die; and application-driven package design (AI, HPC, automotive, HBM, RF systems), and system-level co-design. Large-format substrates processing, including panel warpage control, yield challenges, and process scalability. Advanced IC substrates, including embedded substrate solution, glass core substrate and glass interposer

2. Assembly and Manufacturing: The primary focus of this technical area is process and manufacturing technologies for advanced packaging. Topics include pre-bond wafers preparation includes warpage control and mitigation , backgrinding, thin die handling dicing, plasma dicing, particle reduction process technologies and package assembly processes such as flip chip, wire bonding, thermal compression bonding (TCB), chip stacking, Chip-to-wafer (C2W) fusion/ hybrid bonding, Additional areas of interest include board-level assembly; heat sink and spreader attachment, multi-chip and multi-package integration (SiP, MCP); flexible and printed electronics assembly; assembly yield optimization; The scope further extends Built-in self-test (BIST), burn-in, system-level testing, and high-throughput testing methodologies, which are critical to enabling advanced heterogeneous integration.

3. Electrical Simulation & Characterization: Signal and power integrity, high-speed and RF electrical modeling, electromagnetic simulation, and high-bandwidth interface analysis. Advanced measurement techniques for package and system-level electrical performance, including mmWave, co-packaged optics (CPO), and high-speed data communication systems. Power delivery network (PDN) design and noise suppression for large AI systems.

4. Emerging Technologies: Next-generation packaging for flexible and bioelectronics, MEMS/NEMS, and wide bandgap (SiC, GaN) devices; quantum device packaging including cryogenic integration, low-loss interconnects, qubit scaling, and integration with classical control electronics; and emerging concepts such as neuromorphic and in-memory computing and novel device–package–system co-integration architectures.

5. Interconnection Technologies: Primary focus of this technical domain on interconnect scaling and associated design and implementation challenges that cover materials selection, new processes and equipment capabilities. 1st-level interconnects including wire bonding, flip-chip, TSV, Cu pillar, micro-bumps, thermo-compression bonding (TCB) hybrid bonding, microbump fine-pitch interconnect scaling, and advanced bumpless technologies such as C2W and W2W hybrid bonding, electrical interconnection techniques for high-density integration.

6. Materials and Processing: Substrates (organic core, glass core); build-up films; polymer dielectrics; embedded substrate, lead frames and PCB materials; underfills, encapsulants, and molding compounds; thermal interface materials; novel solder alloys and die-attach materials; wafer and panel-level bonding/debonding materials; conductive adhesives; materials for harsh environments and power device packaging applications; and materials for hybrid bonding and high-power thermal management.

7. Mechanical Simulation & Characterization: Thermo-mechanical stress analysis; fatigue and fracture modeling; moisture sensitivity and diffusion effects; drop, shock, and vibration reliability; process-induced deformation and warpage; and physics-based lifetime prediction models for large and complex packages.

8. Optoelectronics & Display Packaging: Packaging for optical interconnects, fiber coupling and co-packaged optics (CPO). Silicon photonics integration includes PIC packaging, advanced coupling and laser integration, emerging non-silicon photonics platforms (InP, GaAs, SiN, polymer) and heterogenous III-V integration. Integrated electro-optical co-design, thermal and power management supporting applications such as

micro/mini LED, AR/VR displays, and high-density optoelectronic modules.

9. Quality, Reliability & Failure Analysis: Reliability testing at device, package, and board levels, including accelerated life testing and qualification methodologies. Failure mechanisms such as interconnect fatigue, delamination, voiding, and hybrid bonding defects. Advanced diagnostics, inline monitoring, advanced metrology, defect inspection, and FA techniques including X-ray, acoustic, and optical methods.

10. Smart Manufacturing & Equipment Technology: AI/ML-driven manufacturing, smart factories, digital twins, and advanced process control (APC). Equipment innovations for electronic packaging spanning wafer-level, panel-level, and back-end assembly & test, for yield, reliability, and performance optimization. End-to-end data analytics for yield learning, process optimization, fault detection, and predictive maintenance across the entire semiconductor manufacturing value chain

11. Thermal Management & Characterization: Heat dissipation strategies; thermal simulation and measurement; cooling technologies (air, liquid, microfluidic); thermal interface optimization; high-power device cooling; and system-level thermal design for high-power applications and data center

12. Wafer-Level & Panel-Level Packaging: Wafer- and panel-level processes including fan-in/fan-out technologies, redistribution layers (RDL), micro-bumps, TSV and mega-pillars for high-density integration. High-precision pick-and-place, overlay metrology, distortion correction, and alignment control for fine-pitch integration. Test and inspection strategies across wafer-level and panel levels, including known good die (KGD) challenges for chiplet integration.

IMPORTANT DATES

Online abstract submission start	March 31, 2026
Closing of abstract submission	**June 08, 2026**
Notification of acceptance	July 30, 2026
Full Manuscript Submission	**Aug 31, 2026**

Please check the conference website for the latest updates.

ABSTRACT AND PAPER SUBMISSION

You are invited to submit an abstract between 500–750 words long and clearly state the purpose, methodology, results (which must include data, drawings, graphs, or photographs), and conclusions of the work. Additional details on abstract submission can be found on the EPTC website. Abstracts must be received by June 08, 2026. Your submission must have been cleared up by your management and co-authors as applicable and include the authors' affiliations and email addresses. All submissions should be in English, either in pdf or MS Word. Please select the appropriate technical committee for your abstract content from the drop-down list of technical areas so that the right technical committee can evaluate your submission for acceptance. Accepted abstracts will be notified by July 15, 2026. At the technical review committee's or author's discretion, submitted abstracts may be considered for interactive poster presentation. The final manuscript for publication in the conference proceedings is due on September 15, 2026. The conference proceedings are an official IEEE publication, and the accepted papers that are registered and presented (oral and interactive) at EPTC will be uploaded to IEEE Xplore.

BEST PAPER AWARDS

The best oral papers from Academia, Industry and Students will receive cash awards and certificates. A best interactive paper award will also be presented. More details are available on the EPTC website.

CALL FOR INVITED TALKS

You are invited to submit an abstract between 500–750 words long and clearly state the purpose, methodology, results (which must include data, drawings, graphs, or photographs), and conclusions of the work. Abstracts for invited talks must be received by July 31, 2026. Your submission must have been cleared up by your management and co-authors as applicable and include the authors' affiliations and email addresses. All submissions should be in English, either in pdf or MS Word. Abstract should be in 1 of the 12 Electronic Packaging Conference topics. 1 pager bio with a photo embedded needs to be provided along with the abstract for consideration of invited talks. ≥ 10 years of electronic packaging experience in academia/ research institutes/ industry is typically preferred. Abstract for invited talk needs to be directly emailed to techchair@eptc-ieee.net. Acknowledgement will be sent within a day of submission. Abstract for invited talks will be reviewed by the organizing committee and the decision will be notified separately by 31 August 2026. Invited talks are exempted from the full paper submission for publication in the conference proceedings. Invited talks will be scheduled for the first presentation on each track and 30 mins will be assigned for each invited talk. Invited talk needs to be technical in nature and strictly no commercial content.

CALL FOR PROFESSIONAL DEVELOPMENT COURSES

Experts in microelectronics packaging from industry and academia are invited to submit proposals for PDCs to pdcchair@eptc-ieee.net.

CALL FOR EXHIBITORS / SPONSORS

Details of the exhibition and sponsorship opportunities are available on the conference website. For enquiries, please email exhibition@eptc-ieee.net or sponsorship@eptc-ieee.net.

STUDENT TRAVEL GRANTS FOR EPTC

To encourage students in the electronics packaging field to actively participate in the flagship conferences of society, several Student Travel Grants will be offered for EPTC annually. Also, to widen the representation of female students and students from underrepresented countries, at least two grants will be allocated to female student authors and one to a student from a country historically underrepresented at EPTC. Please find details on the EPTC website.

AFFILIATE MEMBERSHIP SUBSIDY PROGRAM

To encourage EPS membership and engagement with EPS, EPS has initiated an Affiliate Membership Subsidy Program whereby non-member conference registrations at EPTC and the other two EPS flagship conferences will be offered complimentary EPS Affiliate Membership for the following year.
Please find details on the EPTC website.

If you have questions about abstract submission, please send your queries at techchair@eptc-ieee.net

For other queries, please email secretariat@eptc-ieee.net

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